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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 1

Complete if known	
Application Number	10/065,920
Filing Date	November 29, 2002
First Named Inventor	Rolf-P. VOLLERTSEN
Art Unit	Not Assigned Yet
Examiner Name	Not Assigned Yet
Attorney Docket Number	01P19578US

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T2
AD		J. H. STATHIS; "Reliability limits for the gate insulator in CMOS Technology"; IBM J. Res. & Dev. Vol. 46 No. 2/3; March/May 2002; Pgs 265-286	
AD		E. Y. WU, E. J. NOWAK, A. VAYSHENKER, W. L. LAI, D. L. HARMON; "CMOS Scaling Beyond the 100-nm Node with Silicon-Dioxide-Based Gate Dielectrics"; IBM J. Res. & Dev. Vol. 46 No. 2/3; March/May 2002; Pgs 287-298	
AD		[illegible] "Thin Gate Oxide Reliability - The Current Status"; Symposium on Nano Device Tech 2001, Taiwan; April 2001	
AD		B. KACZER, R. DEGRAEVE, G. GROESENEKEN, M. RASRAS, S. KUBICEK, E. VANDAMME, G. BADENES; "Impact of MOSFET Oxide Breakdown on Digital Circuit Operation and Reliability"; IEDM Tech Digest 2000; Pgs 553-556	
AD		BARRY P. LINDER, DAVID J. FRANK, KAMES H. STATHIS, STEPHAN A. COHEN; "Transistor-Limited Constant Voltage Stress of Gate Dielectrics"; 2001 Symposium on VLSI Technology Digest of Technical Papers 2001	

Examiner Signature	AD	Date Considered	2/19/04

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